Application Note.

KIC3926S

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1. OVERVIEW

KIC3926S is a current mode PWM controller IC for high performance, low standby power offline flyback converter application, with features of:

1. Few peripheral components

: simplify the peripheral design, reduce the cost.

2. High average efficiency and low standby power dissipation

- quasi-resonant (QR) Mode: switching frequency is low for high efficiency
- light load in QR+PFM mode: efficiency is high
- standby mode: it enters burst mode with low stand-by power dissipation (<75mW), meeting DoE VI requirements.

3. Good consistence in limit power at high/low voltage

: external adjustable peak current compensation according to resistor connected to pin DEM for obtaining the same OCP.

4. No noise

: the minimum frequency is 22kHz, and there is no noise with any load.

5. Various protections

: VCC over voltage protection, over load protection (OLP), leading edge blanking (LEB), primary side over current protection, IC over temperature protection.

2.BLOCK DIAGRAM

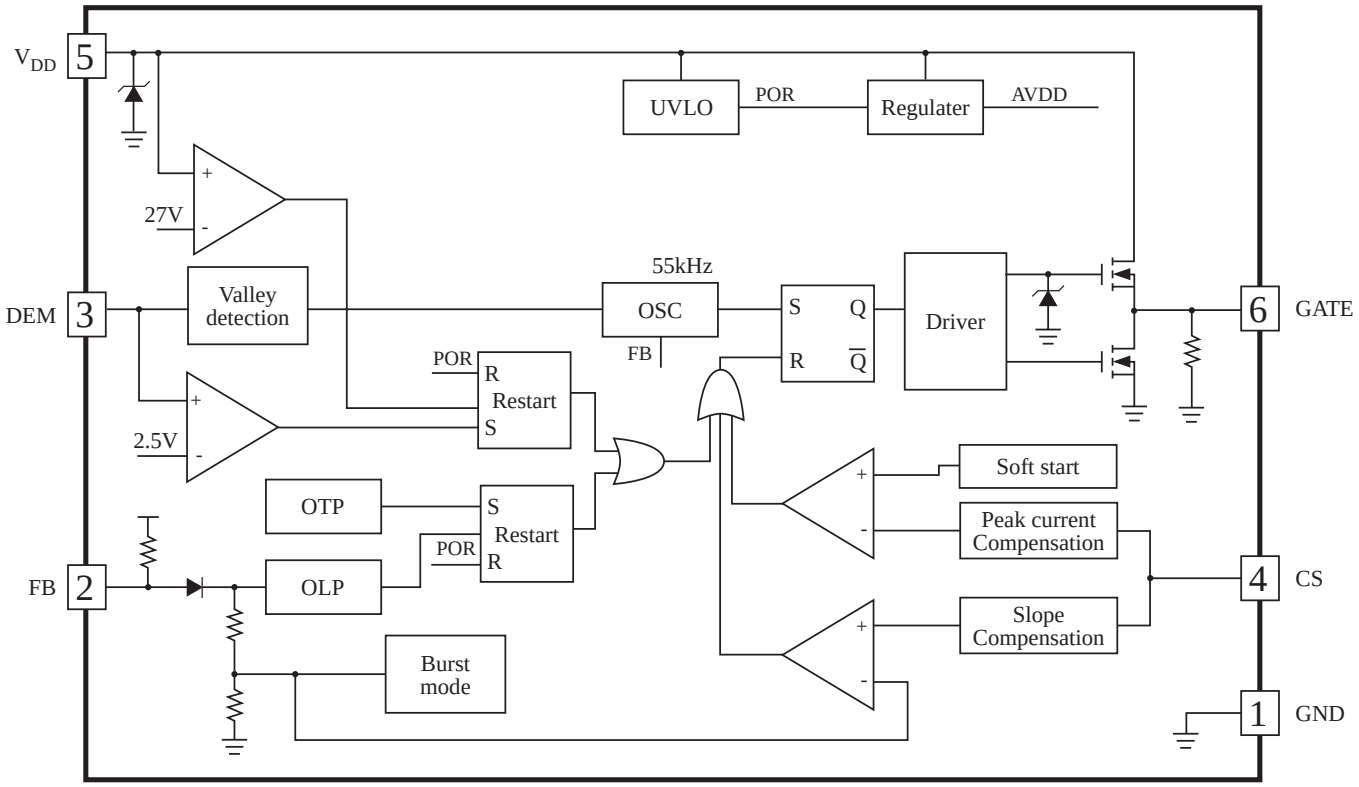


Fig.1 : Block diagram of KIC3926S

Pin No.	Function	Description
1	GND	Ground
2	FB	Feedback input pin
3	DEM	Magnetic core demagnetization detection pin, used for QR Mode detection. Peak current compensation and output overvoltage protection.
4	CS	Current sense input
5	V_{DD}	Power supply pin
6	GATE	Gate driver output pin

3. FUNCTION DESCRIPTION

3.1. Protection and VDD start-up

When FB input voltage is higher than OLP threshold voltage (V_{FB_OL}) and lasts for OLP delay time T_{D_OL}, the circuit enters over-load protection status, and the MOSFET is turned off. Thus the output voltage and V_{DD} decrease. The IC is shutdown to restart if V_{DD} is lower than undervoltage threshold value.
The IC enters V_{DD} over voltage protection if V_{DD} is too high. MOSFET is off and IC restarts.

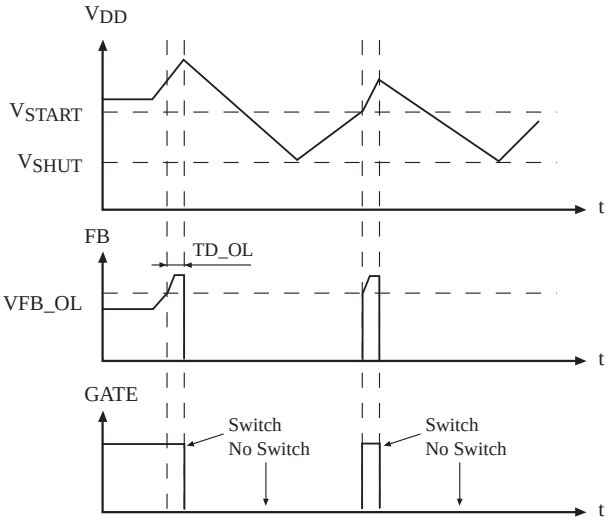


Fig.2 : Over-load protection

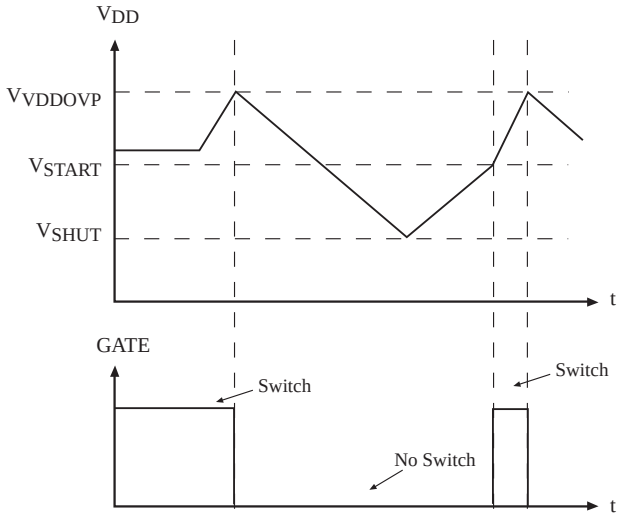


Fig.3 : V_{DD} Over voltage protection

3.2. Frequency-reduced mode

Voltage at pin FB, V_{FB}, will change following the load, as well as the operating mode. There are three operating modes as shown in Fig.5.

1. Normal mode: at the heavy load, V_{FB} is 1.8~4.2V and it works in QR mode with frequency range of 55kHz~69kHz for reducing switching loss. If V_{FB}>4.2V, over-load protection occurs.
2. Frequency-reduced mode: at the light load, V_{FB} is 1.4~1.8V and it works in PFM + QR mode. When input voltage is high, the efficiency can be improved in frequency-reduced mode at 1/4 or half load.
3. Burst mode: at no load or ultra light load, V_{FB} is 0.9~1.0V and it enters burst mode for reducing standbypower dissipation.

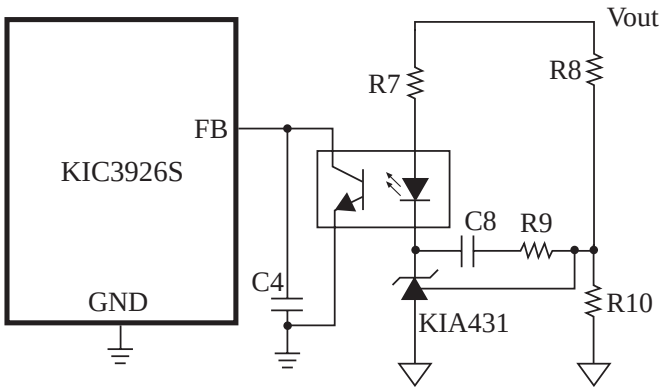


Fig.4 : FB Application circuit

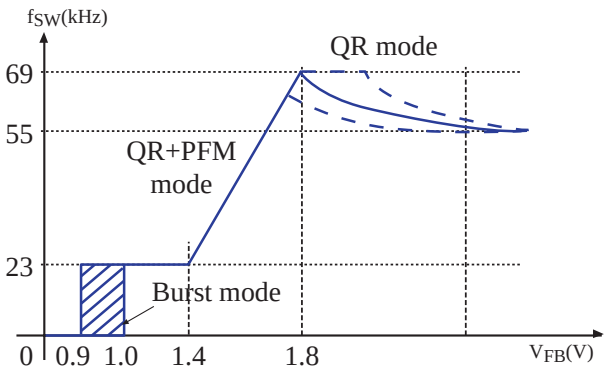


Fig.5 : f_{SW} vs. V_{FB}

Note : C4 should be placed as close as possible to IC

3.3. Limit power compensation

External adjustable peak current mode is adopted. The input voltage is judged by measuring current at pin DEM, and the peak current is compensated corresponding to the result. And the external resistance can be adjusted for keeping consistency of peak current with different input voltage.

Reduce the pull-up resistance connected to pin DEM when OCP value increases with the increasing input voltage, and vice versa.

4. APPLICATION IN FLYBACK CIRCUIT

4.1. Typical application circuit

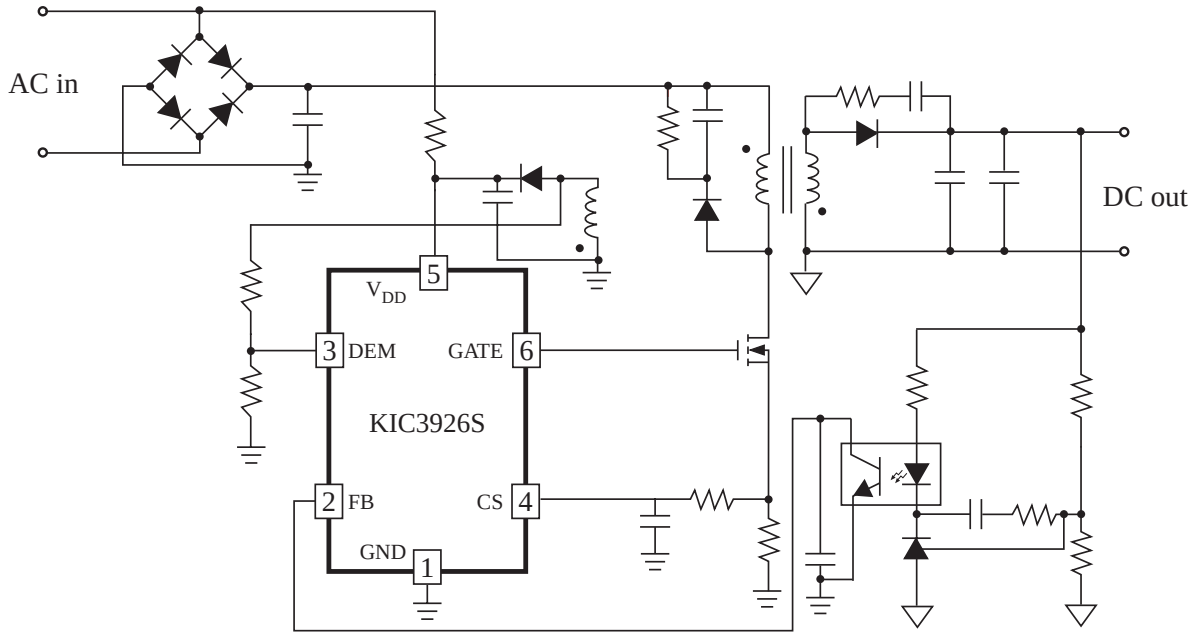


Fig.6 : Typical applicaion in flyback circuit

4.2. Transformer design

4.2.1 Determining V_{OR}, D_{MAX} and n

When Q is on, the voltage on the primary winding, V_P, (it is up to 375V when input voltage is 265V). When the primary winding number of turns is N_P; and the secondary winding number of turns is N_S; then the turns ratio is described as below:

$$n = \frac{N_P}{N_S}$$

And secondary voltage is given by:

$$V_S = \frac{V_{DC}}{n}$$

As the diode on the secondary side is reversed, there is no current through the secondary winding. The voltage stress of the diode is calculated:

$$V_{ODI} = \frac{V_P}{n} + V_O$$

Where VO is the output voltage.
When Q is off, the energy stored in transformer is released. The voltage on the secondary winding is:

$$V_S = V_F + V_O$$

Where, V_F is the forward voltage drop of the diode.
Primary winding voltage is:

$$V_P = nV_S + V_{LK} = V_{OR} + V_{LK}$$

where V_{LK} is the spike voltage caused by leakage inductance and V_{OR} is reflected voltage.
Then voltage on MOSFET is given by:

$$V_{DS} = V_{DCMAX} + V_{OR} + V_{LK}$$

Actually, 20~50V margin should be taken into consideration for application and V_{LK} is generally 100~120V and V_{OR} is 80~90V for 600V MOSFET.
Duty cycle in CCM:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

And switching period is described as:

$$T_{SW} = T_{ON} + T_{OFF}$$

Based on volt-second balance principle, the following equation can be derived

$$V_{DC} * T_{ON} = V_{OR} * T_{OFF}$$

Where T_{ON} is the turn-on time of MOSFET, while T_{OFF} is the turn-off time.
Consequently, the maximum duty cycle at the lowest AC input voltage is as follows,

$$D_{MAX} = \frac{V_{OR}}{V_{DCMIN} + V_{OR}}$$

Usually D_{MAX} is 0.3~0.5
And the turns ratio is :

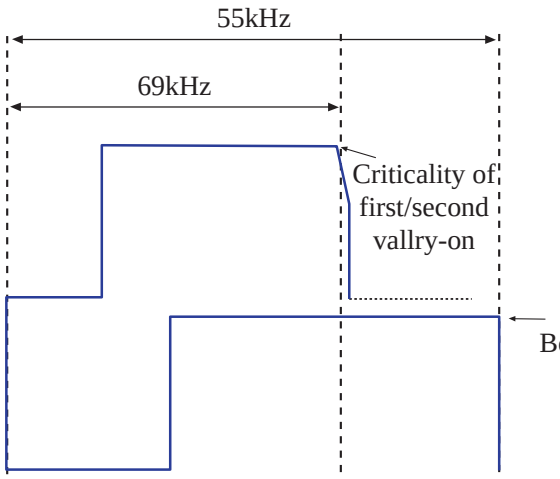
$$n = \frac{V_{OR}}{V_O + V_F}$$

4.2.2. Primary inductance L_P

1. KIC3926S works in QR + PFM mode. Valley-Mode switching is adopted for reducing switching loss,which greatly increases the efficiency with full load or 3/4 load at high input voltage. Thus it is recommended to turn on the switch at the first valley while full load at 230VAC input with universal input voltage.

2. L_p calculation: the highest switching frequency is 69kHz and the lowest is 55kHz at normal mode. The inductance is limited by these two frequencies to turn on at the first valley, as shown in Fig. 7, where,
   -Lp : primary winding inductance, the unit is mH
   -n : turns ratio
   -V_O : output voltage, the unit is V
   -V_{DC} : Rectified DC voltage, the unit is V, V_{DC}=230V*1.414=325V
   -P_O : output power, the unit is W
   -f_{SW} : switching frequency, the unit is kHz
   - η : efficiency.

   Then the maximum primary inductance, $L_{P1}$and minimum inductance L_{P2} can be given, and the average value is L_p=0.5*(L_{P1}+L_{P2})



$$P_O = \frac{1}{2} L_P I_{PK}^2 f_{SW} \eta$$

$$I_{PK} = \frac{V_{DC}}{L_P} DT_{SW}$$

$$D = \frac{nV_O}{nV_O + V_{DC}}$$

$$\Downarrow$$

$$L_P = \frac{(nV_O V_{DC})^2 \eta}{2P_O (nV_O + V_{DC})^2 f_{SW}}$$

Figure 7. Switching waveform and the formula in QR mode

3. Tiny adjustment of inductance is necessary to turn on at the first valley and guarantee margin in mass production. Test the whole machine with trsndformer whose inductance is $L_P=0.5*(L_{P1}+L_{P2})$ at 230V, then measure the first current I_1 when the converter operates in critical continuous current mode from the first valley, and the second current I_2 when it enters the second valley. If $I=0.5*(I_1+I_2)$ is larger than I_O (current with full load), L_P should be increased, and vice versa.

4. In QR mode, the operating frequency at low input voltage and full load is 55kHz. The following equation is used to verify whether it is saturated.

$$B_{MAX} = \frac{L_P \times I_{PK}}{N_P \times A_e}$$

-B_{MAX} : the maximum magnetic flux density
-L_p : primary winding inductance, uH
-I_{PK} : primary peak current, A
-A_e : core effective cross sectional area, mm^2. . Generally
-B_{MAX} is lower than 0.3T and 0.25T is recommended considering the temperature affect.

4.2.3. Peak current compensation and output overvoltage protection

As shown in Fig.8, the voltage divider resistors are connected to auxiliary winding and GND, pin DEM is the multi-function pin. When MOSFET is on, the voltage on the auxiliary winding is negative and the voltage at pin DEM is clamped to 0V. The current flowing from pin DEM to auxiliary winding and the current value is related to the input voltage. Consequently, the peak current compensation at different input voltage can be calculated corresponding to the current.

1. R_A and R_B are calculated as the following equation, where K=0.067, R_{COMP}=24kΩ, ΔV_{COMP}=0.12V, N_A is the auxiliary winding number of turns. Suppose $R_A : R_B = 10 : 1$

$$R_A = \frac{K \Delta V_{DC} N_A}{N_P \Delta V_{COMP}} R_{COMP}$$

2. Determine R_A. R_A should be adjusted for the consistency of OCP at different input voltage as shown in Fig.8. If OCP curve is up (2), R_A should be reduced. While OCP curve is down (3), R_A should be increased.

Determine R_B. Pin DEM acts as output voltage sense pin when MOSFET is off. It enters OVP if DEM voltage is higher than the threshold value 2.5V and the output overvoltage protection voltage is determined by the ratio of R_A and R_B. OVP should not be occurred during OVP setting.

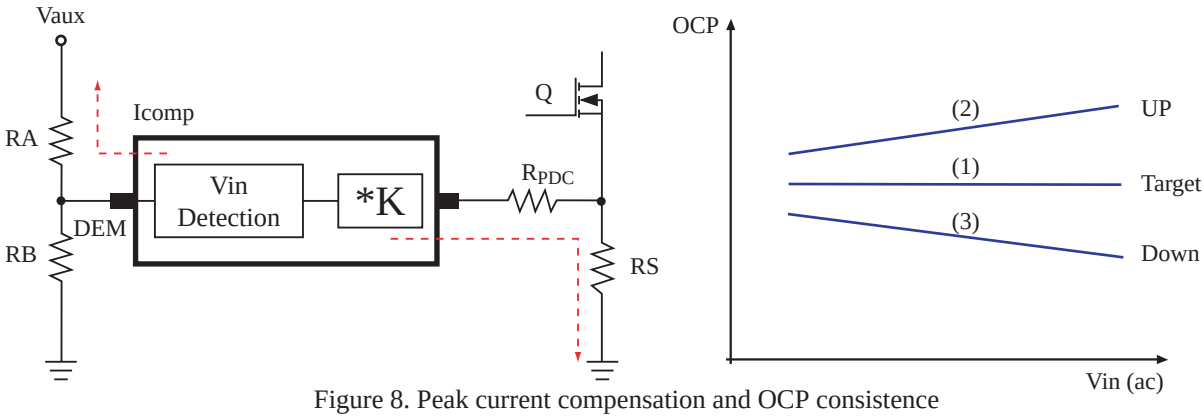


Figure 8. Peak current compensation and OCP consistence

4.3. Key component selection

4.3.1. Capacitor

The bus capacitor C_{IN} is selected according to 2uF/W rule. If the hold time after power cut is required, the capacitor is given as follows,

$$C_{IN} = \frac{2P_O T_{HOLD}}{\eta (V^2_{MIN} - V^2_{OFF})}$$

Where, $-P_O$: output power
- η : output efficiency
- T_{HOLD} : hold time
- V_{MIN} : min. voltage
- V_{OFF} : off voltage.

The output capacitor is decided by output voltage ripple, ΔV_O, which is described as:

$$\Delta V_O = \Delta I_O * ESR$$

Where, $-\Delta V_O$: the output voltage ripple
- ΔI_O : the output current ripple
- ESR : equivalent serial resistance of the output capacitor.

If ESR is too large, LC filter, the corner frequency of which is 1/10~1/5 of switching frequency, can be applied.

4.3.2. MOSFET

MOSFET is decided by the peak voltage when primary winding MOSFET is off and peak current when primary winding MOSFET is on. As described above,

$$V_{DS} = V_{INMAX} + V_{OR} + V_{LK}$$

And the RMS primary current is given by:

$$I_{PRMS} = \sqrt{D_{MAX}\left(I^{2}_{PK} - I_{PK}I_{PRPL} + \frac{I^{2}_{PRPL}}{3}\right)}$$

Meanwhile, the package and heatsink should be taken into consideration. The surface temperature of MOSFET should be lower than 110¡C in normal operation.

4.3.3. Secondary output diode

The secondary diode is also determined by the current stress, which is equal to the output current, and voltage stress given as follows. Usually 10% margin for the voltage stress is necessary and the rated current of the selected diode is twice the maximum average current.

The secondary diode is determined by tha maximum reverse voltage V_{RRM}, forward average current I_{FAV}, forward voltage drop V_F and thermal resistance $R_{\theta JC}$.
When Q is on, secondary diode is reversed and the maximum reverse voltage is given by:

$$V_{ODIMAX} = \frac{V_{DCMAX}}{n} + V_O$$

Where, $-V_{DCMAX}$: DC voltage of the maximum input AC voltage. Usually, V_{ODIMAX} should be less than V_{RRM}. Rated forward current of diode should be 2 times of OCP threshold value. The forward voltage drop V_F and thermal resistance $R_{\theta JC}$ should be as low as possible.

4.3.4. Start-up resistor and start-up capacitor

After power on, the capacitor connected to pin V_{DD} is charged through the start-up resistor till V_{DD} rises to the start-up voltage, V_{START}(typ. 15.5V). Then it is powered by the auxiliary winding. The start delay time T_{DELAY} is decided by this process.
Start-up resistor connection after the rectifier bridge is a common application as shown in Fig. 9, which is stable and easy to calculate the start-up time, while the standby power dissipation is high.

$$T_{DELAY\_MAX} = R_{ST}C_{VDD}\ln\left(\frac{V_{DCMIN} - I_{VDD\_ST}R_{ST}}{V_{DCMIN} - I_{VDD\_ST}R_{ST} - V_{START}}\right)$$

Where, $-V_{START}$: V_{DD} start up voltage

$-I_{VDD\_ST}$: start up current

$-R_{ST}$: start up resistor

$-C_{VDD}$: start up capacitor

Generally, the startup delay should be less than 2s. Another startup way is connecting the startup resistor before the rectifier bridge, as shown in Fig.10. C2 and D2 are added and the stand-by power dissipation is lower. In comparison with the first connection way, RST is constant, while C1 is about 1/10 of C_{VDD} and the input high voltage on startup resistor decreases by a half. Thus the power dissipation on startup resistor reduces to 1/4.

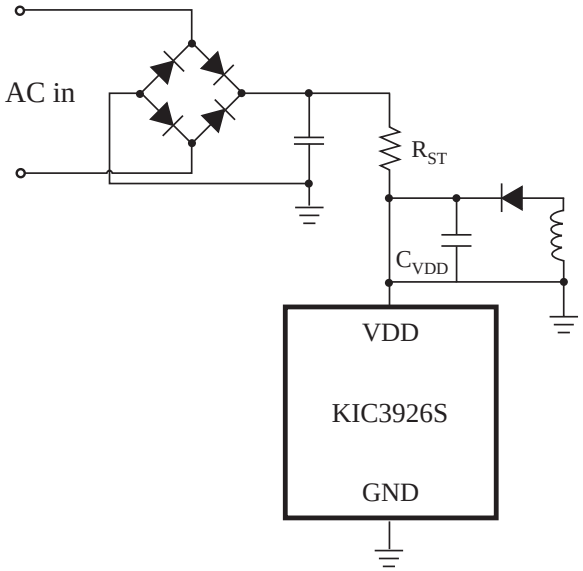


Figure 9. Start-up resistor after rectifier bridge

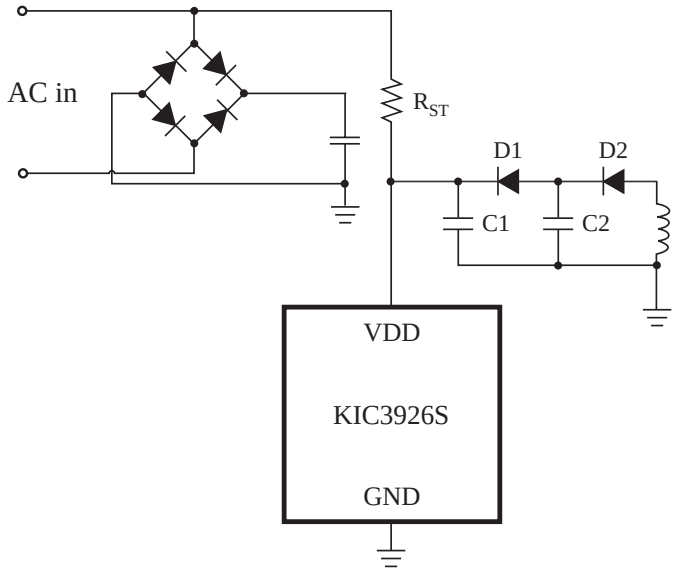


Figure 10. Start-up resistor before rectifier bridge

4.4. Performance optimization

4.4.1. Stand-by power dissipation

Methods for reducing stand-by power dissipation:

1. Apply two-stage start-up and connect start-up resistor to AC L or N line.
2. Decrease VDD at no load (12V is recommended) for reducing IC power dissipation.
3. Increase OCP for enlarge Burst period at no load. Operating frequency should not be in the range of 2~4kHz to avoid abnormal sound.
4. Increase pull-up resistor for opto-coupler to reduce the operating current.

4.4.2. System efficiency

Loss is caused by MOSFET, IC, primary absorbing circuit, secondary output diode, common-mode inductor, etc. The following are recommends for increasing efficiency:

1. Select schottky diodes with low forward voltage drop.
2. Select capacitors with low ESR.
3. Apply multi strand wire for secondary winding in consideration of skin effect and reduce primary turns if possible to decrease leak inductance loss.
4. Adjust the inductance to obtain the on at the first valley for QR mode to reduce loss.
5. Increase the resistor or reduce the capacitor of the primary absorbing circuit.

4.4.3. EMI design

1. Reduce couplings. Minimize the loop area of the bus capacitor, transformer and MOSFET, as well as Rs loop, the loop area of the transformer, secondary output diode and output filter capacitor.
2. Reduce EMI noise induced. Power transistor and transformer are the dominated noise source. The absorbing circuit is used to reduce di/dt and dv/dt for decreasing EMI noise from the transistor, including RCD absorbing circuit on the primary side and RC absorbing circuit in parallel with the secondary output diode. Another way to reduce the noise of the primary MOSFET is decreasing the driver current. In order to reduce noise from the transformer, shielding winding or copper film can be applied.
3. Optimize EMI filter design. Differential-mode inductor and X-capacitor are used for suppressing differential-mode noise, while common-mode inductor and Y-capacitor are adopted for suppressing common-mode noise.
4. Decrease the noise on MOSFET. Noise with frequency of 30-50MHz maybe caused by fast switching of MOSFET and this can be decreased by increasing driver resistance/ primary RCD absorbing circuit, adopting low frequency MOSFET in auxiliary winding and

4.4.4. Reduce MOSFET voltage stress

Voltage stress on MOSFET should not be larger than 90% of rated value in design and it can be reduced as follows:

1. Reduce turns ratio of the primary and secondary windings.
2. Apply sandwich winding in the transformer to reduce leakage inductance.
3. Optimize absorbing circuit, including using damped resistor and slow-recovery diode.

4.4.5. Start-up with capacitive load

It is necessary to start-up with heavy capacitive load in some applications, where the output voltage increases slowly and V_{FB} maintains to be high. If the duration time exceeds the over-load delay time 90ms, OLP occurs. To improve capacitive load driving capability:

1. Increase limit output power by regulating the transformer primary inductance.
2. Extend the rise time of V_{FB} by modifying the parameters of the feedback loop to increase energy transferring time.
3. Place the auxiliary winding close to the primary winding to increase coupling.

4.4.6. PCB design

1. Safety distance: distance should be longer than 2.5mm between the fuse and L\N line, and longer than 6.5 mm between the primary and secondary windings, referring to IEC-60950.
2. Loop: areas of AC loop, PWM loop, rectified loop and filtering loop should be as small as possible. That is, power device should be placed as close as possible and power line (AC lines, positive lien.GND) should be close.
3. Place IC close to MOSFET, as well as the surrounding components, especially for components connecting directly to IC.
4. Adopt single-point grounding in the PWM loop. Connect the GND for components surrounding controller IC to GND of IC before connecting to S of MOSFET, which is then connected to negative of the bus capacitor. As shown in Fig.11, connect GND for components surrounded IC to G3 first, then connect to G4 and G1. Connect G6, G2 and G5 to G1 separately. The sensitive signals, such as the feedback signal through the opto-coupler, current sensing signal, should be far away from the noise source.

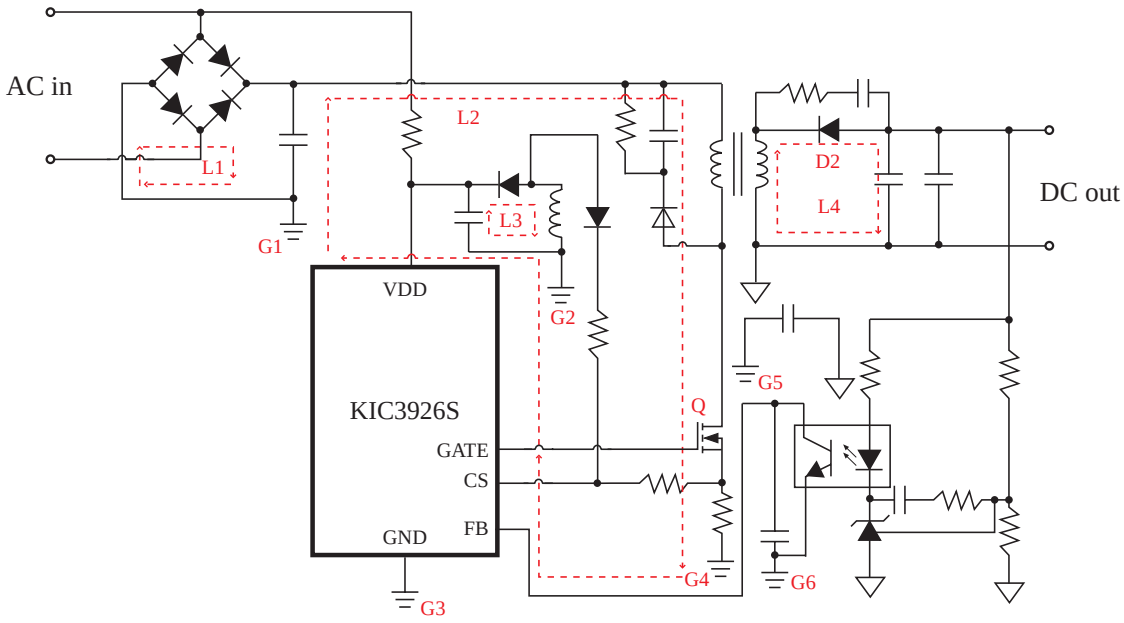


Figure 11. Layout loop